ABSTRACT OF THE DISCLOSURE

A network node (5) including a line card (20) for packet-based data communications is disclosed. The line card (20) includes a transmit FIFO buffer (24T) and a receive FIFO buffer (24R), for buffering communications within the line card (20). Each of the buffers (24T, 24R) operate in a dual-port fashion, receiving asynchronous read and write requests, for reading data words from and writing data words to the buffers (24T, 24R). The buffers (24T, 24R) each include a memory array (45) of conventional single port random access memory cells, for example static RAM cells. Clock cycles are assigned by the buffers (24T, 24R) as internal read and internal write cycles, in alternating fashion. A write buffer (42) receives input data words, and schedules a double-data-word write to the memory array (45) upon receiving a pair of input data words, in the next internal write cycle. A read request buffer (44) receives read strobes, or read enable signals, from a downstream function, and upon receiving two such strobes, schedules the read of a double-data-word from the memory array (45). By converting the asynchronous read and write requests into scheduled reads and writes, respectively, the buffers (24T, 24R) operate as dual-port FIFO buffers.